
# Amandeep Singh

PhD (VI Year II Semester)
Ph.D. Electronics and Communication Engineering
Contact No: 9501286656
Email: a_singh@ece.iitr.ac.in
Registration No: 20915002/2026

Indian Institute of Technology Roorkee


**VERIFIED**

## Area of Interest

Memory Design, In-Memory Computation, Chip tapeout & Testing

## Education

| Year | Degree/Examination | Institution/Board | CGPA/ Percentage |
|---|---|---|---|
| 2026 | Ph.D. | Indian Institute of Technology, Roorkee | 8.429 |
| 2020 | Postgraduate (PG) | Punjab Engineering College (Deemed to Be University) Chandigarh | 8.740 |
| 2014 | Graduate (UG) | Guru Gobind Singh College of Modern Technology, Kharar, Punjab | 82.60 % |
| 2010 | Intermediate (Class XII) | Central Public Senior Secondary School, Ghoman, PSEB Board | 70.44 % |
| 2008 | Matriculate (Class X) | S.G.H.K.Public School, Ghoman, PSEB Board | 72.70 % |

## Internships

**Embedded System** | Centre for Development of Advanced Computing (C-DAC Mohali) January 2014 - July 2014

- Project title: Design and Development of an Embedded-Based Quiz Game

## Projects

**Time-Domain-Based In-Memory Computation Architecture (TD-IMC) for XAC and Multibit MAC Operations** | Indian Institute of Technology Roorkee January 2024 - June 2024

- Chip Tape-Out: Fabricated at TSMC Taiwan using the 65 nm technology node.
- Tools Used: Cadence Virtuoso, HSPICE, Xilinx Vivado, Synopsys Design Compiler (DC), and IC Compiler (ICC).
- Architecture: Introduced a specialized voltage-controlled delay cell (VCDC) for performing XNOR/Multiplication operations and achieved accumulation by cascading VCDC cells to obtain XAC/MAC.
- Advantages: The same architecture was utilized to achieve both robust 4-bit MAC and XAC operations. The proposed IMC does not require area- and power-hungry DACs, ADCs, or capacitors.
- Simulation Results: Achieved 1711 GOPS throughput for XAC, 112.4 GOPS for MAC, 544.07 TOPS/W for XAC, 15.04 TOPS/W for MAC, and 99.22% MNIST accuracy.
- Application: XAC (XNOR and accumulation) operations are fundamental in various computational tasks, especially in binary neural networks (BNNs).

**PVT-Insensitive Time-Domain-based In-Memory Computation with Improved Linearity for Binary Neural Networks** | Indian Institute of Technology Roorkee September 2022 - April 2023

- Chip Tape-Out: Fabricated at TSMC Taiwan using the 65 nm technology node.
- Tools Used: Cadence Virtuoso, HSPICE, Xilinx Vivado, DC, and IC Compiler.
- Architecture: Proposed a time-domain-based in-memory computation (TD-IMC) architecture to perform XNOR-and-accumulation (XAC) operations using two types of delay cells: XNOR and delay cell (XDC) and PVT-insensitive XNOR-and-delay cell (PXDC). The PVT-insensitive XNOR-and-delay cell (PXDC) is a PVT-tolerant cell that includes the XDC and an array of controllable load capacitors to compensate for PVT variations. The XAC operations are performed serially.
- Advantages: PXDC-based architecture achieved similar XAC results across different process corners and temperatures. The proposed XAC-based IMC architecture improves linearity, signal margin, and energy efficiency and provides robust XAC operation.
- Simulation Results: The signal margin mean is 116.5 ps with a standard deviation of 7.64 ps, extracted from 1000 Monte Carlo process variations. The classification accuracy achieved on MNIST test images is 99.6%, and the Differential Non-Linearity (DNL) is found to be +0.10/-0.25 LSB. This work achieved a throughput of 1057 GOPS for XDC and 3.01 GOPS for PXDC-based IMC architecture. The energy efficiency achieved is 673 TOPS/W for XDC and 13.12 TOPS/W for PXDC-based IMC architecture.

**Area-Efficient In-Memory Computation with Improved Linearity using Voltage-Controlled Delay Cell-based Ring Oscillator** | Indian Institute of Technology Roorkee May 2023 - September 2023

- Tools Used: Cadence Virtuoso, HSPICE, Xilinx Vivado, DC, and IC Compiler.
- Architecture: Proposed an in-memory computation (IMC) architecture utilizing a 128x128 6T-SRAM array with a specialized delay cell for multiplication and accumulation (MAC) operations. The delay cells are cascaded to form a ring oscillator (RO), converting the MAC value to the RO frequency, which is measured by a simple digital counter.
- Advantages: The proposed IMC does not require area- and power-hungry DACs, ADCs, TDCs, or capacitors.
- Simulation Results: Post-layout simulations in a 65 nm process achieved 10.32/1321.2 GOPS throughput, 30.3/49.5 TOPS/W energy efficiency for serial/parallel row access, and 99% classification accuracy on MNIST images.
- Application: MAC operations are fundamental in various computational tasks, especially in machine learning and neural networks.

**Develop an analog propeller clock using an LED strip** | Indian Institute of Technology Roorkee
October 2020 - January 2021

- Principle: The fundamental concept behind this clocks operation is the persistence of vision (POV).
- Microcontroller: Tiva C Launchpad TM4C123GH6PM.
- Approach: The systems circuitry is rotated at such a high speed that it creates the illusion of a continuous analog clock to the human eye.

**Design of Two-Stage Op-amp** | Indian Institute of Technology Roorkee October 2020 - December 2020

- Technology Node & Supply Voltage: 180nm CMOS technology, 1.8 Volts
- Tools used: Cadence Virtuoso
- Simulation Results: Gain: 80.65 dB, UGB: 125.86 MHz, Phase Margin: 40.34 degree, CMRR: 86.35 dB, Slew Rate: 0.94 V/ns, Power: 251.84 uW

**Analysis of Low-Power High-Speed Dynamic Comparator** | Punjab Engineering College, Chandigarh
September 2019 - September 2020

- Objective: Analyzed different dynamic comparators to reduce delay and power dissipation.
- Tools and Technology Node Used: Cadence Virtuoso, 180 nm CMOS technology
- Simulation Results: Single-tail comparator: 11.49 uW power, 58.67 ns delay; Double-tail comparator: 14.82 uW power, 130.2 ns delay (0.8V supply).

**Design and Development of an Embedded-Based Quiz Game** | Centre for Development of Advanced Computing (C-DAC) Mohali January 2014 - July 2014

- Objective: Develop a compact and affordable quiz game.
- Hardware: AT89C51 microcontroller, 20x4 LCD, 74573 MUX, keyboard, power supply.
- Advantages: Area efficient, low power consumption, portable, cost-effective.
- Application: Suitable for quiz competitions in schools, colleges, and other venues.

**Accelerating Secure Hash Algorithm 3 (SHA-3) using In-Memory Computation** | Indian Institute of Technology Roorkee January 2025 - April 2025

- Chip Tape-Out: Chip is under fabrication at TSMC Taiwan using the 65 nm technology node (May-2025).
- Tools Used: Cadence Virtuoso, HSPICE, Xilinx Vivado, Synopsys Design Compiler (DC), and IC Compiler (ICC).
- Architecture:This work presents an In-memory architecture for implementing the Secure Hash Algorithm-3, which aims to accelerate the computation of hash digest.
- Advantages: A 5-input in-memory XOR operation was proposed to reduce the latency.
- The operations XOR and Rotation were fused so that they could be computed in the same cycle, reducing the latency.
- The read-compute-store (RCS) scheme was incorporated into the design to eliminate the need to latch the computed output before storing it in the memory.
- Simulation Results:The proposed architecture can work with the clock with a frequency of 500 MHz and provide 2388 clock cycles latency to compute the hash of a single message block. This yields a throughput of 192 Mbps.
- Application: Data Integrity Verification, IoT & Embedded Systems, Cloud Storage Validation.

## Awards / Scholarships / Academic Achievements

- Awarded a financial grant from the Science and Engineering Research Board (SERB) and IEEE Circuits and Systems Society (CAS) for participation at the IEEE International Symposium on Circuits and Systems (ISCAS-2024) in Singapore from May 19, 2024, to May 22, 2024.
- Teaching assistant in the course Digital System Design (FPGA-based design) taught by Prof. Bishnu Prasad Das, Department of ECE, IIT Roorkee. This course is broadcast on the Coursera platform.
- Transcribing files of course VLSI Physical Design With Timing Analysis offered by IIT Roorkee on the NPTEL platform
- Awarded the fellowship for attending VLSID-2024 Conference
- GATE Qualified: 2019 (gate score 645, AIR 1517); 2018 (gate score 446, AIR 4438)
- GATE Qualified 2017 (gate score 598, AIR 2667)
- The best digital IC tapeout award at VLSID 2025 in Bengaluru
- The best digital IC tapeout award at VLSID 2026 in Pune

## Skills

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|---|---|
| Computer languages | HSPICE, Verilog, SystemVerilog, VHDL, TCL, Python, C++. |
| Software Packages | Cadence Virtuoso, Design Compiler, IC Compiler, LTspice, Xilinx Vivado, TensorFlow, Matlab |
| Additional Courses | Digital VLSI Circuit Design Digital System Design Semiconductor Memories Memory Design & Testing Soft Computing-Machine Learning Analog VLSI Circuit Design |
| Languages Known | English, Hindi, Punjabi |

## Positions of Responsibility & Extra Curriculars

**Authors** | IEEE International Symposium on Circuits and Systems (ISCAS) May 2024

- I delivered a technical presentation on my research paper, PVT-Insensitive Time-Domain-based In-Memory Computation with Improved Linearity for Binary Neural Networks, on May 22, 2024, at the RWS Convention Centre in Singapore.

**Authors** | IEEE International Symposium on Smart Electronic Systems (IEEEiSES)-2023 December 2023

- I delivered a technical presentation on my research paper, Area-Efficient In-Memory Computation with Improved Linearity using Voltage-Controlled Delay Cell-based Ring Oscillator, on December 20, 2023, at Nirma University, Ahmedabad.

**Attendees** | VLSI Design-2024 January 2024

- 37th International Conference on VLSI Design and 23rd International Conference on Embedded System Design (VLSID 2024) at ITC Royal Bengal, Kolkata, India.

**Attendees** | VLSI Design-2021 February 2021

- 34th International Conference on VLSI Design and the 20th International Conference on Embedded Systems (VLSID)

**Attendees** | IEEE International Symposium on Integrated Circuits and Systems (ISICAS 2024) October 2024

- I have presented my PhD research work titled, "PVT-Insensitive Time Domain-Based In-Memory Computation with Improved Linearity for Machine Learning Applications" in the IEEE Circuit and Systems Society Workshop on "Semiconductors for All: From Silicon to Systems" held in New Delhi, India on October 20, 2024.

**Attendees** | 39th International Conference On VLSI Design (VLSID-2026) January 2026

- I have presented our tapeout results on "A Configurable Time-Domain In-Memory Computing Macro for Multi-Bit MAC and Binary XAC Operations in Edge AI Devices" at VLSID 2026, held from 5th7th January 2026 at JW Marriott, Pune. This work won the Best Digital Tapeout Award, recognizing its innovative time-domain compute architecture for energy-efficient edge AI devices.

## Research Publications

- A. Singh and B. P. Das, "PVT-Insensitive Time-Domain-based In-Memory Computation with Improved Linearity for Binary Neural Networks", in IEEE International Symposium on Circuits and Systems (ISCAS), Singapore, Singapore, 2024, doi: 10.1109/ISCAS58744.2024.10558168., 2024
- P. K. Saragada, S. Manna, A. Singh and B. P. Das, "A Configurable 10T SRAM-Based IMC Accelerator With Scaled-Voltage-Based Pulse Count Modulation for MAC and High-Throughput XAC", in IEEE Transactions on Nanotechnology, doi: 10.1109/TNANO.2023.3269946., 2023
- A. Singh and B. P. Das, "Area-Efficient In-Memory Computation with Improved Linearity using Voltage-Controlled Delay Cell-based Ring Oscillator", in IEEE International Symposium on Smart Electronic Systems (iSES), Ahmedabad, India, doi: 10.1109/iSES58672.2023.000, 2023
- A. Singh and B. P. Das, "Dual- VTH XDC-Based Time-Domain In-Memory Computing Architecture with PVT-Insensitive XAC Operations for BNN Applications", in IEEE Transactions on Very Large Scale Integration (VLSI) Systems (submitted), ID TVLSI-00772-2025, 2025
- A. Singh and B.P.Das, "CTD-IMC: A Configurable Time-Domain-Based In-Memory Computation using Voltage-Controlled Delay Cell for MAC and XAC", in IEEE Transactions on Circuits and Systems I: Regular Papers (Communicated), TCAS-I-00838-2026, 2026

## References

**Dr. Bishnu Prasad Das**
Professor
Indian Institute of Technology, Roorkee
bishnu.das@ece.iitr.ac.in
+91-1332-28479